

**Introduction:**

There have been numerous requests from our customers to reduce the test time of the PCT450 application. The current application takes approximately 11 seconds per socket to test. The test program incorporates many software delays to insure that the software will work with a wide variety of host socket controllers and host systems. However, in most cases many of these delays are unnecessary. Beginning with version 1.19 of the PCT450 application, the user will be given the option to reduce many of these delays through command line switches.

**Options Switch:**

Beginning with release 1.19 of the PCT450 software, a new command line switch allows the user to modify certain internal parameters. Future versions of software may have additional options to control certain parameters.

The syntax of the new switch is as follows:

**-mX:Y**

With "-m" as the command, followed by a one or two-digit parameter number "XX" and an integer parameter "Y". The -mX:Y parameter can be placed anywhere on the command line after the PCT450 command. Several -mX:Y parameters may appear on the same command line.

**Parameter Description:**

- m0 : 1**      Enables test timer. Will printout the number of seconds that the PCT450 program takes to test a socket.
- m1 : 1**      Reduced address test enable. Address pattern test reduced to a walking 1 and walking 0 pattern. (default is disabled)
- m2 : x**      Specifies the settling delay for the VPP power supplies. When the Vpp tests are enabled (-tx option) the PCT450 software will delay approximately 550ms after the Vpp levels are switched to allow the voltages to settle. In most case the actual settling time is much shorter. The user can specify the settling time in DOS timer ticks (55ms/tick). In most cases a setting of 2 (110ms) is acceptable.
- m3 : x**      Specifies the delay between when the Host controller chip is initialized and the when the command to apply power is sent to the chip. The default value is approximately 2 seconds. However, in most cases this can be reduced to 0.
- m4 : x**      Specifies the delay between the power-on command to the chip and when the PCCtest card starts to be accessed. The default delay is approximately 2 seconds for TI and Ricoh controllers and 2.55 seconds for O2 controllers. In many cases this can be reduced to less than 1 second.

**Example:**

The following examples show the possible test time improvement for a TI PCI1131 chip with the specified delay times:

- |        |  |
|--------|--|
| Test 1 | Normal operation with time display - 10.6 seconds<br><code>PCT450 -b63 -v -0 -m0:1</code>              |
| Test 2 | Reducing the Address/Data pattern test - 8.35 seconds<br><code>PCT450 -b63 -v -0 -m0:1 -m1:1</code>    |
| Test 3 | Reducing the A/D settling delays to 110mS - 8.79 seconds<br><code>PCT450 -b63 -v -0 -m0:1 -m2:2</code> |
| Test 4 | Reducing the power-on delays - 8.08 seconds<br><code>PCT450 -b63 -v -0 -m0:1 -m3:2 -m4:17</code>       |
| Test 5 | All of the above - 3.30 seconds<br><code>PCT450 -b63 -v -0 -m0:1 -m1:1 -m2:2 -m3:2 -m4:17</code>       |