SYCARD TECHNOLOGY

PCCextend 100 User's Manual

Preliminary

M200001-00
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1.0 Introduction

Sycard Technology's PCCextend 100 PCMCIA extender card is a debug tool for PCMCIA development and test. PCCextend offers the following features:

- PCCswitch simulates card removal/insertion cycle
- Low profile design compatible with type I, II and III sockets
- 4 layer construction to insure low noise environment
- All 68 pins available as test points
- Both I/O and memory mode signals clearly marked
- Vcc, Vpp1 and Vpp2 can be isolated through jumper blocks for current measurements
- Surface mount resistors and/or capacitors can be added to any signal line
- Vcc LEDs indicate 3.3V or 5V operation
- Convenient grounding posts for scope probes or other test equipment

2.0 Using the PCCextend 100

Using the PCCextend is relatively straightforward. The extender card is inserted into the desired slot in the host system. Then the PC Card under test is inserted into the card connector.

Caution: Insertion and removal of the extender and PC card should be done with care. The PC Card's fragile connectors may be broken or bent if improper force is used. Both card and extender should be inserted straight without any lateral movement or force. Proper care and use of the extender card will insure years of trouble free operation.

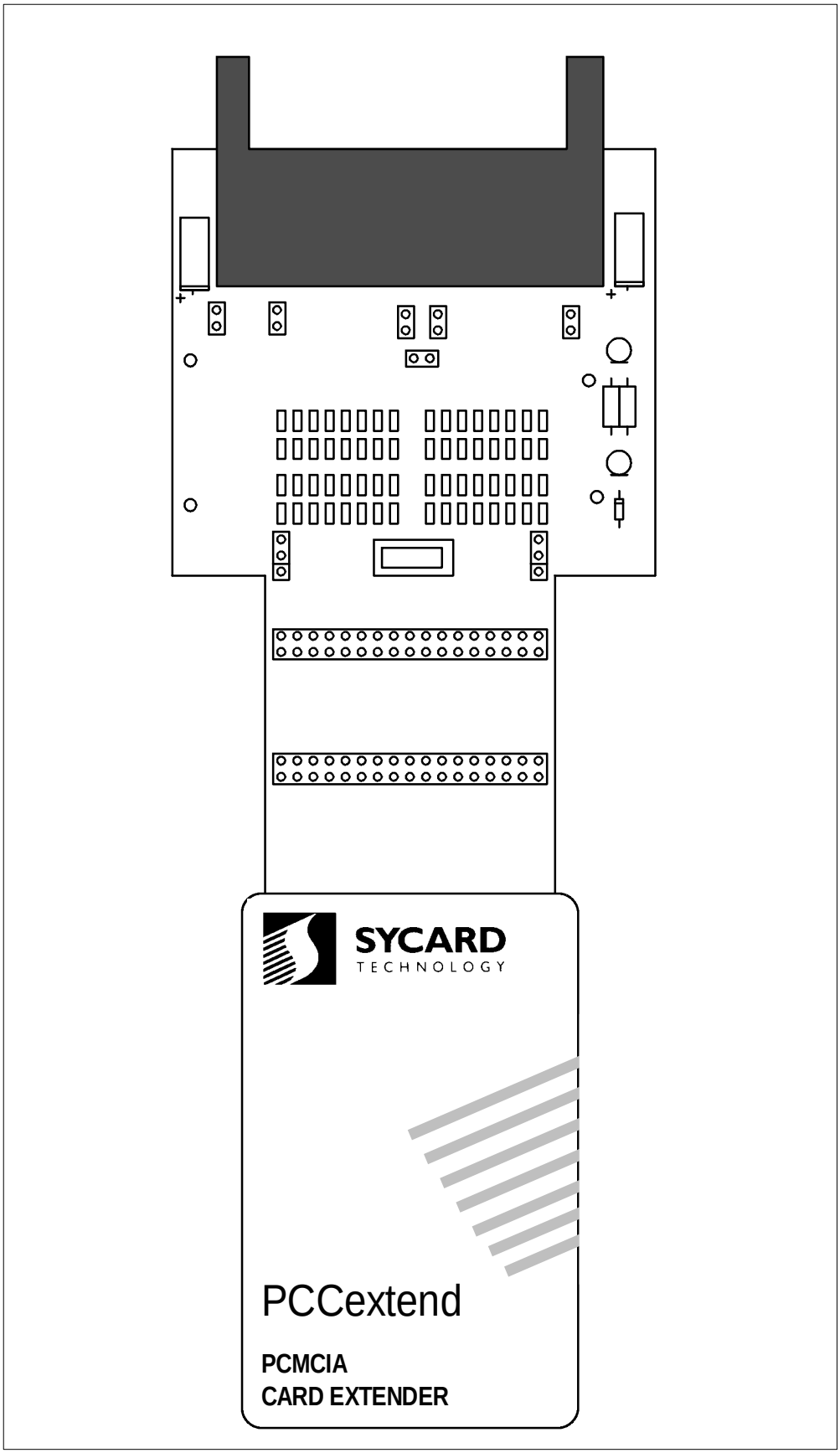
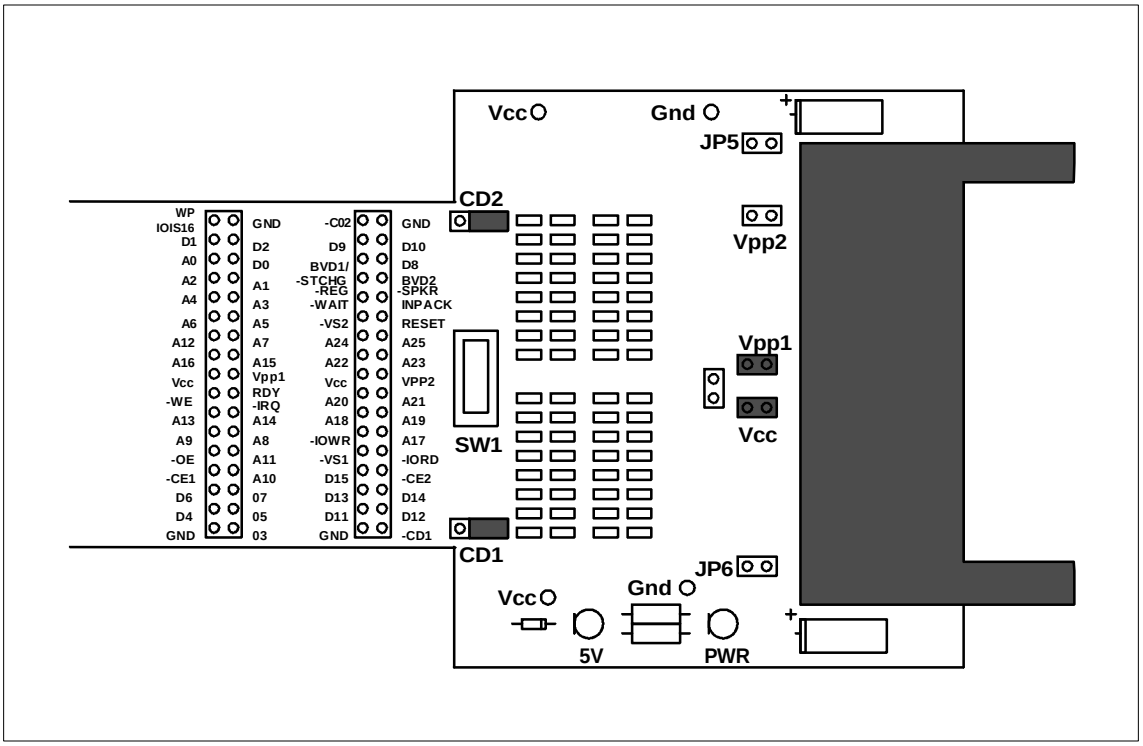


Figure 2.0-1 The PCCextend 100

2.1 Test points

All 68-pins of the interface are available to probe through clearly marked headers.



2.2 Power Indicators

Two LED power indicators display the status of the socket's Vcc. The PWR LED indicates that power is applied to the board. When both the PWR LED and the 5V LED are lit, a Vcc of greater than approximately 3.5V is present. When only the PWR LED is lit, the Vcc is at a level of less than 3.5V.

Note: The power LEDs are designed to indicate the presence of power on the Vcc supply pins. The LEDs do not provide an accurate measurement of Vcc. Use a voltmeter to determine the actual operating voltage.

2.2 Current Measurements

Vcc, Vpp1 and Vpp2 power buses may be isolated from the PC Card socket through three sets of jumper blocks. Each jumper block consists of two sets of jumpers. Both jumpers must be removed to isolate the power. A current meter can be inserted to measure card current consumption.

Caution: Care must be taken to insure that the current measuring device is inserted before turning on power to the host socket. Improper power sequencing may cause a damaging latchup condition.

2.3 Using the PCCswitch

PCCextend 100 includes the PCCswitch, which can be used to momentarily interrupt the CD1 and CD2 signals. The PCCswitch is centrally located on the PCCextend 100 between the termination area and test points. When properly configured, the PCCswitch can interrupt the card detect signals (-CD1 and -CD2) to simulate a card removal/insertion cycle. Two three pin headers are used to configure the PCCswitch. When both CD1 and CD2 headers are in the "A" position, CD1 and CD2 are routed directly from the host socket to the PCCextend socket.

When the jumpers are in this position the PCCswitch is not in the circuit. In the "B" position, the host socket's CD1 and CD2 is routed through the PCCswitch to the CD1 signal on the PCCextend socket. When a card is inserted, CD1 and CD2 may be momentarily interrupted by pressing the PCCswitch.

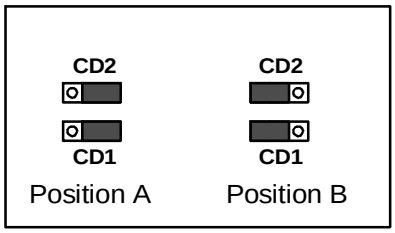


Figure 2.3-1 Card Detect Switch

To test the operation of the PCCswitch, be sure that your PC Card Software drivers are loaded. Momentarily press the PCCtest switch. Most software drivers will issue a removal beep followed by an insertion beep. The software may also remove power from the socket when the card is removed.

2.4 Termination and Prototype Area

A termination area located between the test points and the card connector allows access to all PC Card signals. A series of surface mount pads allows the user to add series resistors, pull-down resistor, or capacitance to any signal. The SMT pads are arranged as follows:

When shipped from the factory, the resistor pads are shorted with PCB traces. In order to insert series resistor, these traces must be cut prior to soldering the resistor to the board. Pull-down resistors may be inserted by adding a resistor to the corresponding SMT capacitor pad. Filter capacitors may be added by inserting a small capacitor into the corresponding SMT capacitor pad. Figure 2.4-1 and 2.4-2 illustrate the termination areas located on both sides of the PCCextend board. Use this guide when making modifications to the board, since the silk-screen designations may be difficult to read.

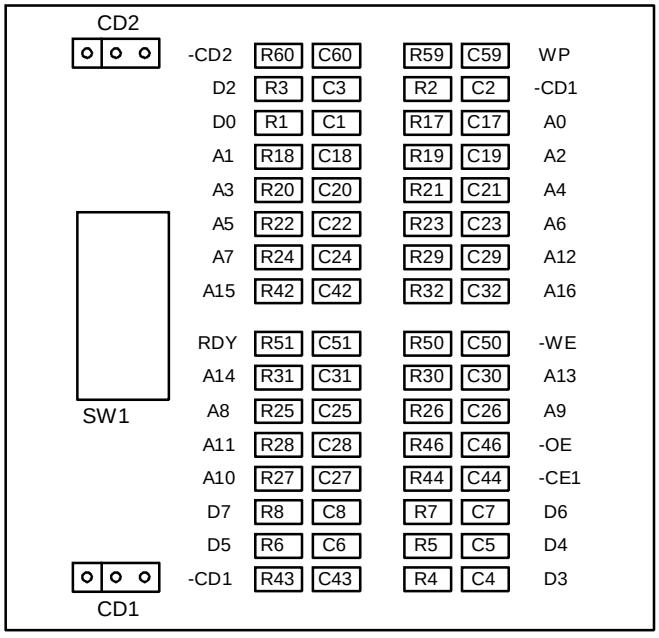


Figure 2.4-1 Termination Area - Component Side

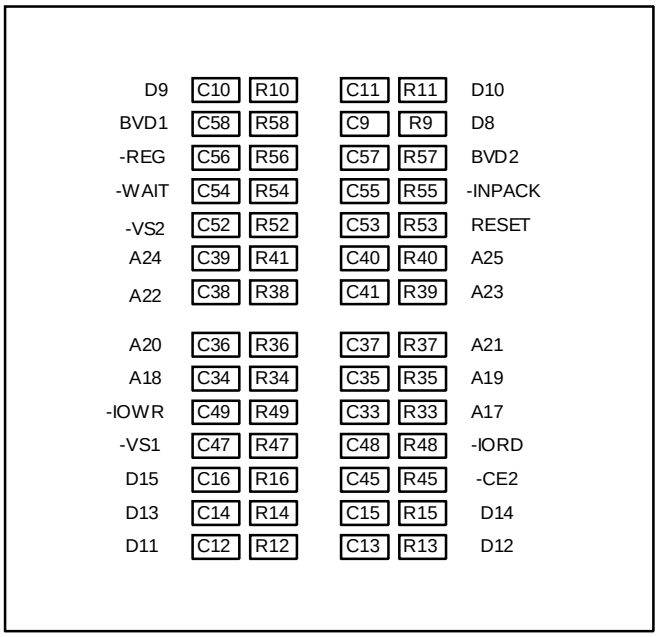


Figure 2.4-2 Termination Area - Solder Side

2.5 PCCextend Current Protection Device

A resettable fuse protects the host from excessive current consumption from the card. Located at R61, the, PolySwitch resettable fuse provides low resistance operation up to 900mA. The PolySwitch fuse may be by passed by soldering a shorting wire across JP4.

Appendix

A. PC Card 68-Pin Interface

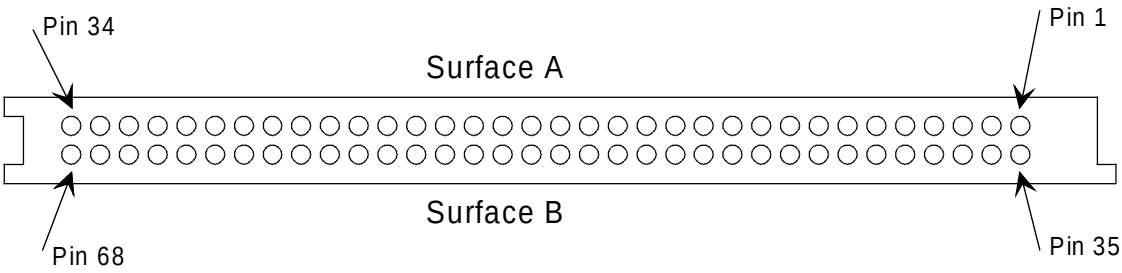
PC Card Pinout - Memory Mode

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	35	GND	Ground
2	D3	Data Bit 3	36	CD1#	Card Detect 1
3	D4	Data Bit 4	37	D11	Data Bit 11
4	D5	Data Bit 5	38	D12	Data Bit 12
5	D6	Data Bit 6	39	D13	Data Bit 13
6	D7	Data Bit 7	40	D14	Data Bit 14
7	CE1#	Card Enable 1	41	D15	Data Bit 15
8	A10	Address Bit 10	42	CE2#	Card Enable 2
9	OE#	Output Enable	43	VS1#	Voltage Sense 1
10	A11	Address Bit 11	44	RFU	Reserved
11	A9	Address Bit 9	45	RFU	Reserved
12	A8	Address Bit 8	46	A17	Address Bit 17
13	A13	Address Bit 13	47	A18	Address Bit 18
14	A14	Address Bit 14	48	A19	Address Bit 19
15	WE#	Write Enable	49	A20	Address Bit 20
16	READY	Ready/Busy	50	A21	Address Bit 21
17	VCC	Card Power	51	VCC	Card Power
18	VPP1	Programming Supply Voltage 1	52	VPP2	Programming Supply Voltage 2
19	A16	Address Bit 16	53	A22	Address Bit 22
20	A15	Address Bit 15	54	A23	Address Bit 23
21	A12	Address Bit 12	55	A24	Address Bit 24
22	A7	Address Bit 7	56	A25	Address Bit 25
23	A6	Address Bit 6	57	VS2#	Voltage Sense 2
24	A5	Address Bit 5	58	RESET	Card Reset
25	A4	Address Bit 4	59	WAIT#	Extend Bus Cycle
26	A3	Address Bit 3	60	RFU	Reserved
27	A2	Address Bit 2	61	REG#	Register Select
28	A1	Address Bit 1	62	BVD2	Battery Voltage Detect 2
29	A0	Address Bit 0	63	BVD1	Battery Voltage Detect 1
30	D0	Data Bit 0	64	D8	Data Bit 8
31	D1	Data Bit 1	65	D9	Data Bit 9
32	D2	Data Bit 2	66	D10	Data Bit 10
33	WP	Write Protect	67	CD2#	Card Detect 2
34	GND	Ground	68	GND	Ground

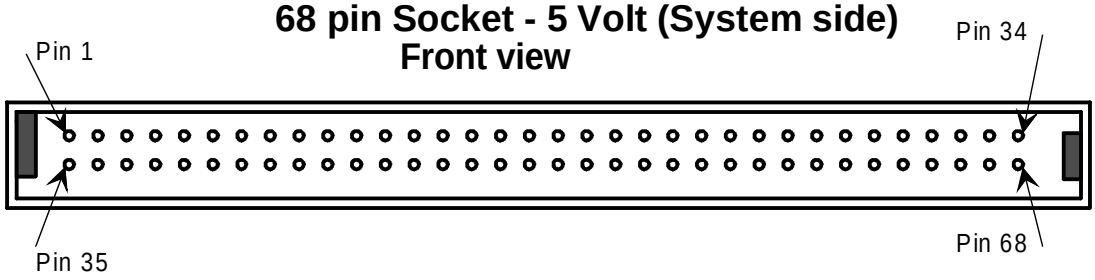
PC Card Pinout - I/O Mode

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	35	GND	Ground
2	D3	Data Bit 3	36	CD1#	Card Detect 1
3	D4	Data Bit 4	37	D11	Data Bit 11
4	D5	Data Bit 5	38	D12	Data Bit 12
5	D6	Data Bit 6	39	D13	Data Bit 13
6	D7	Data Bit 7	40	D14	Data Bit 14
7	CE1#	Card Enable 1	41	D15	Data Bit 15
8	A10	Address Bit 10	42	CE2#	Card Enable 2
9	OE#	Output Enable	43	VS1#	Voltage Sense 1
10	A11	Address Bit 11	44	IORD#	I/O Read Strobe
11	A9	Address Bit 9	45	IOWR#	I/O Write Strobe
12	A8	Address Bit 8	46	A17	Address Bit 17
13	A13	Address Bit 13	47	A18	Address Bit 18
14	A14	Address Bit 14	48	A19	Address Bit 19
15	WE#	Write Enable	49	A20	Address Bit 20
16	IREQ#	Interrupt Request	50	A21	Address Bit 21
17	VCC	Card Power	51	VCC	Card Power
18	VPP1	Programming Supply Voltage 1	52	VPP2	Programming Supply Voltage 2
19	A16	Address Bit 16	53	A22	Address Bit 22
20	A15	Address Bit 15	54	A23	Address Bit 23
21	A12	Address Bit 12	55	A24	Address Bit 24
22	A7	Address Bit 7	56	A25	Address Bit 25
23	A6	Address Bit 6	57	VS2#	Voltage Sense 2
24	A5	Address Bit 5	58	RESET	Card Reset
25	A4	Address Bit 4	59	WAIT#	Extend Bus Cycle
26	A3	Address Bit 3	60	INPACK#	Input Port Acknowledge
27	A2	Address Bit 2	61	REG#	Register and I/O select enable
28	A1	Address Bit 1	62	SPKR#	Digital Audio Waveform
29	A0	Address Bit 0	63	STSCHG#	Card Status Changed
30	D0	Data Bit 0	64	D8	Data Bit 8
31	D1	Data Bit 1	65	D9	Data Bit 9
32	D2	Data Bit 2	66	D10	Data Bit 10
33	IOIS16#	IO Port is 16 bits	67	CD2#	Card Detect 2
34	GND	Ground	68	GND	Ground

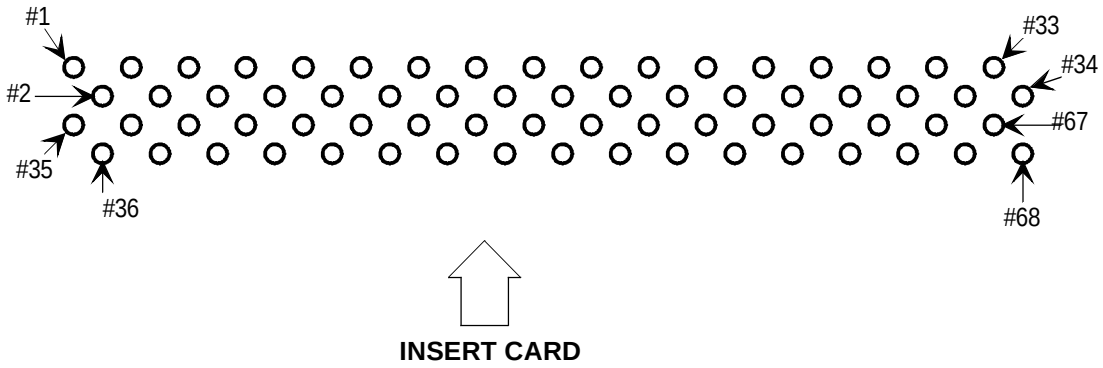
68 pin Card Side Connector - 5 Volt



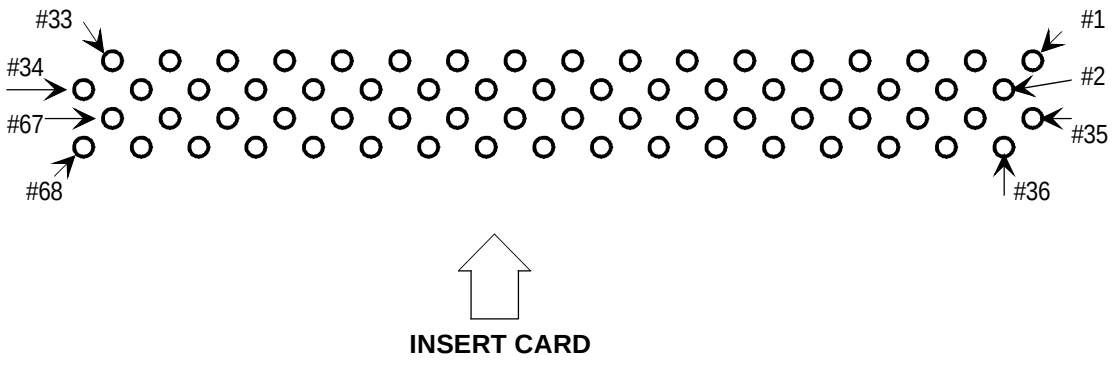
68 pin Socket - 5 Volt (System side)
Front view



Right angle connector hole pattern - Top side

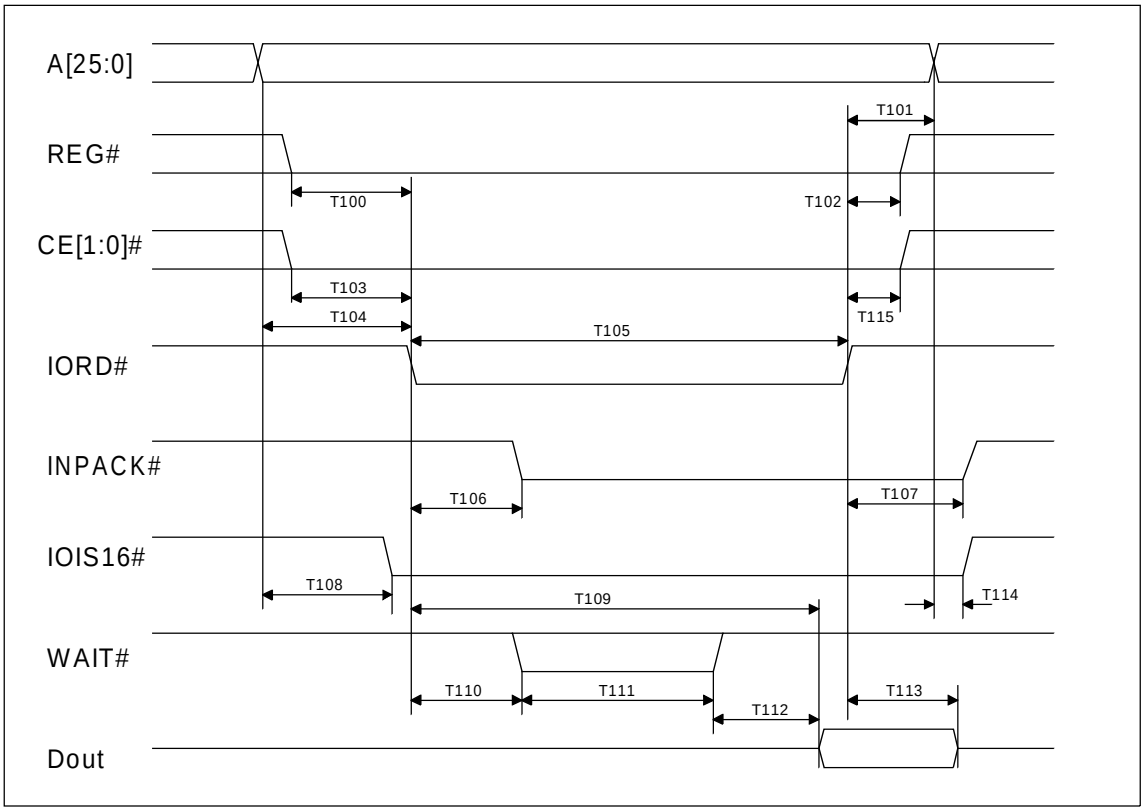


Right angle connector hole pattern - Bottom Side



B. PC Card Timing Reference

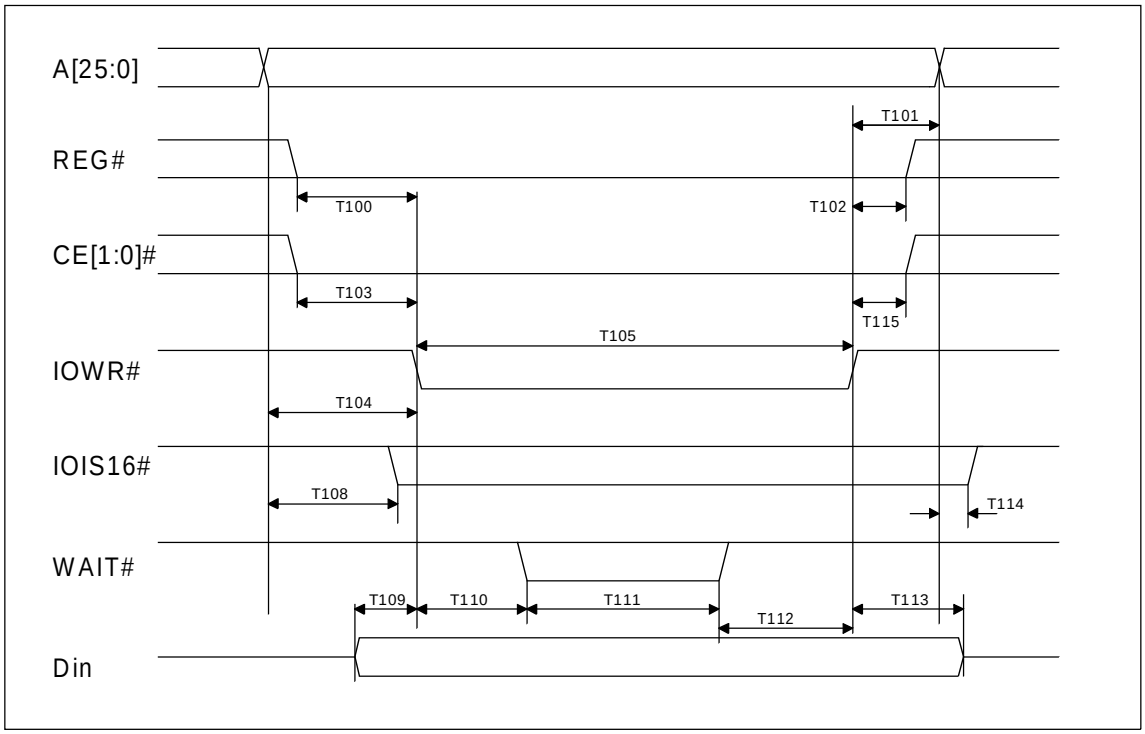
B.1 I/O Read Timing



I/O Read Timing

Ref	Symbol	Description	Min	Max
T100	tsuREG	REG# setup to IORD#	5ns	
T101	thA	Address hold after IORD# de-asserted	20ns	
T102	thREG	REG# hold after IORD# de-asserted	0ns	
T103	tsuCE	CE# to IORD# setup time	5ns	
T104	tsuA (IORD)	Address setup before IORD#	70nS	
T105	twIORD	IORD# strobe width	165ns	
T106	tdfINPACK	INPACK# delay from IORD# active	0ns	45ns
T107	tdrINPACK	INPACK# delay from IORD# inactive		45ns
T108	tdfIOIS16	IOIS16# delay from Address valid		35ns
T109	td (IORD)	Data Valid after IORD#		100ns
T110	tdWT	IORD# to WAIT# delay		35ns
T111	tw	WAIT# width		12us
T112	td (WT)	Data Valid after WAIT# inactive		0ns
T113	th (IORD)	Data hold after IORD# de-asserted	0ns	
T114	tdrIOIS16 (ADR)	IOIS16# delay from address invalid		35ns
T115	thCE	CE# hold after IORD# inactive	20ns	

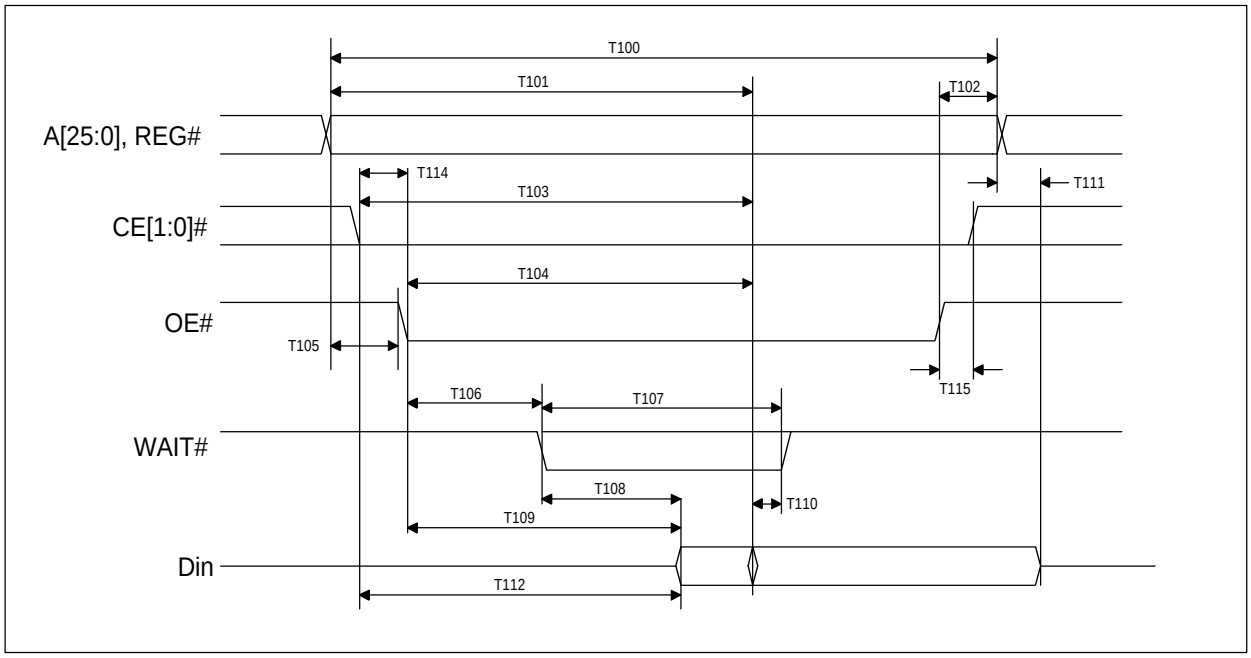
B.2 I/O Write Timing



I/O Write Timing

Ref	Symbol	Description	Min	Max
T100	tsuREG (IOWR)	REG# setup to IOWR#	5ns	
T101	thA (IOWR)	Address hold after IOWR# de-asserted	20ns	
T102	thREG (IOWR)	REG# hold after IOWR# de-asserted	0ns	
T103	tsuCE (IOWR)	CE# to IOWR# setup time	5ns	
T104	tsuA (IOWR)	Address setup before IOWR#	70nS	
T105	twIOWR	IOWR# strobe width	165ns	
T108	tdfIOIS16	IOIS16# delay from Address valid		35ns
T109	tsu (IOWR)	Data Setup before IOWR#	60ns	
T110	tdWT (IOWR)	IOWR# to WAIT# delay		35ns
T111	tw WT	WAIT# width		12us
T112	tdr IOWR (WT)	WAIT# deasserted to IOWR# deasserted	0ns	
T113	th (IOWR)	Data hold after IOWR# de-asserted	30ns	
T114	tdrIOIS16 (ADR)	IOIS16# delay from address invalid		35ns
T115	thCE(IOWR)	CE# hold after IOWR# de-asserted	20ns	

B.3 Memory Read Timing

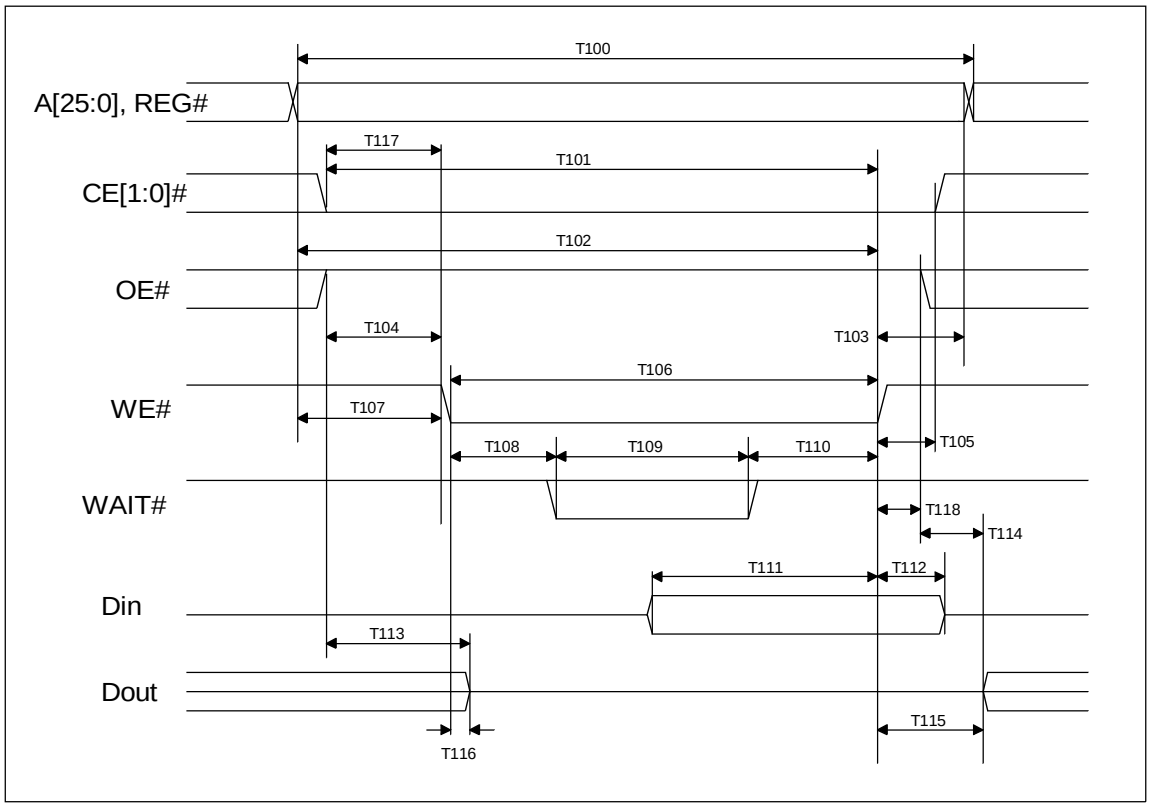


Memory Read Timing

Ref	Symbol	Description	600ns		250ns	
			Min	Max	Min	Max
T100	tcR	Read Cycle Time	600ns		250ns	
T101	ta(A)	Address access time		600ns		250ns
T102	th (A)	Address hold time	35ns		20ns	
T103	ta (CE)	CE# access time		600ns		250ns
T104	ta (OE)	OE# access time		300ns		125ns
T105	tsu (A)	Address setup time	100ns		30ns	
T106	tv (WT-OE)	WAIT# Valid from OE#		100ns		35ns
T107	tw (WT)	WAIT# Pulse width		12us		12us
T109	ten (OE)	Output enable time from OE#		5ns		5ns
T110	tv (WT)	Data setup for WAIT# released	0ns		0ns	
T111	tdis (OE)	Output disable inactive to data float		150ns		100ns
T112	ten(CE)	Output enable time from CE#		5ns		5ns
T114	tsu(CE)	CE# setup time	0ns		0ns	
T115	th(CE)	CE# hold after OE# inactive	35ns		20ns	

Note: All timing for 250ns accesses to common memory. 600ns cycle times apply for 3.3V operation.

B.4 Memory Write Timing

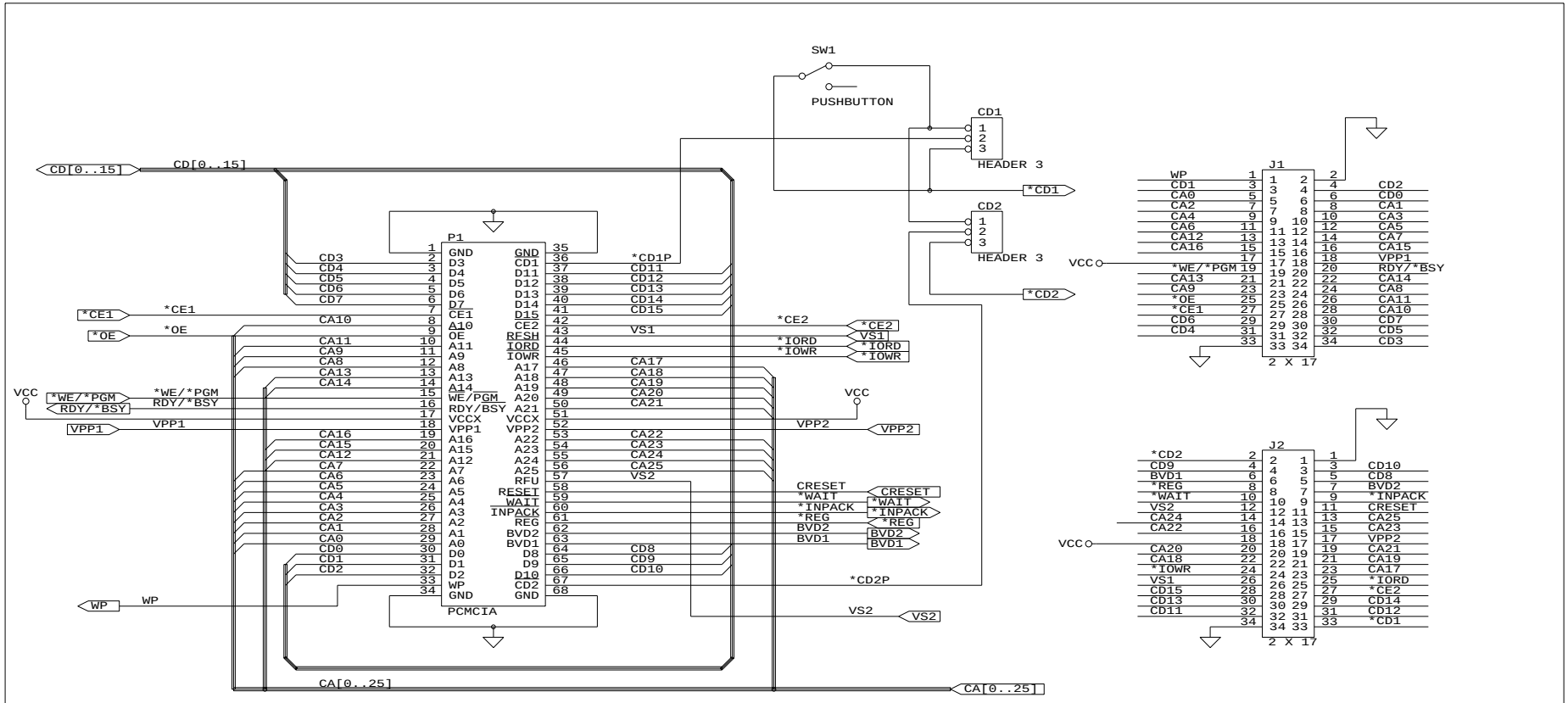


Memory Write Timing

Ref	Symbol	Description	600ns		250ns	
			Min	Max	Min	Max
T100	tcW	Write cycle time	600ns		250ns	
T101	tsu(CE - WEH)	CE# active to WE# high	300ns		180ns	
T102	tsu(A-WEH)	Address valid to WE# high	350ns		180ns	
T103	trc(WE)	Write recover time	70ns		30ns	
T104	tsu(OE-WE)	Output enable setup OE# to WE#	35ns		10ns	
T105	th(CE)	CE# hold time	35ns		20ns	
T106	tw(WE)	WE# pulse width	300ns		150ns	
T107	tsu(A)	Address setup time	50ns		30ns	
T108	tv(WT-WE)	WAIT# valid from WE# active		100ns		35ns
T109	tw(WT)	WAIT# pluse width		12us		12us
T110	tv(WT)	WE# high from WAIT# inactive	0ns		0ns	
T111	tsu(D-WEH)	Data setup time	150ns		80ns	
T112	th(D)	Data hold time	70ns		30ns	
T113	tdis(OE)	Output disable time from OE# inactive		150ns		100ns
T114	ten(OE)	Output enable time from OE# active	5ns		5ns	
T115	ten(WE)	Output enable time from WE# inactive	5ns		5ns	
T116	tdis(WE)	Output disable from WE# active		150ns		100ns
T117	tsu(CE)	CE# setup time	0ns		0ns	
T118	th(OE-WE)	Output enable hold from WE#	35ns		10ns	

Note: All timing for 250ns speed version. 600ns cycle times apply for 3.3V operation. See PC Card Standard for other speed versions.

C. PCCextend 100 Schematic



HOST SIDE CONNECTOR

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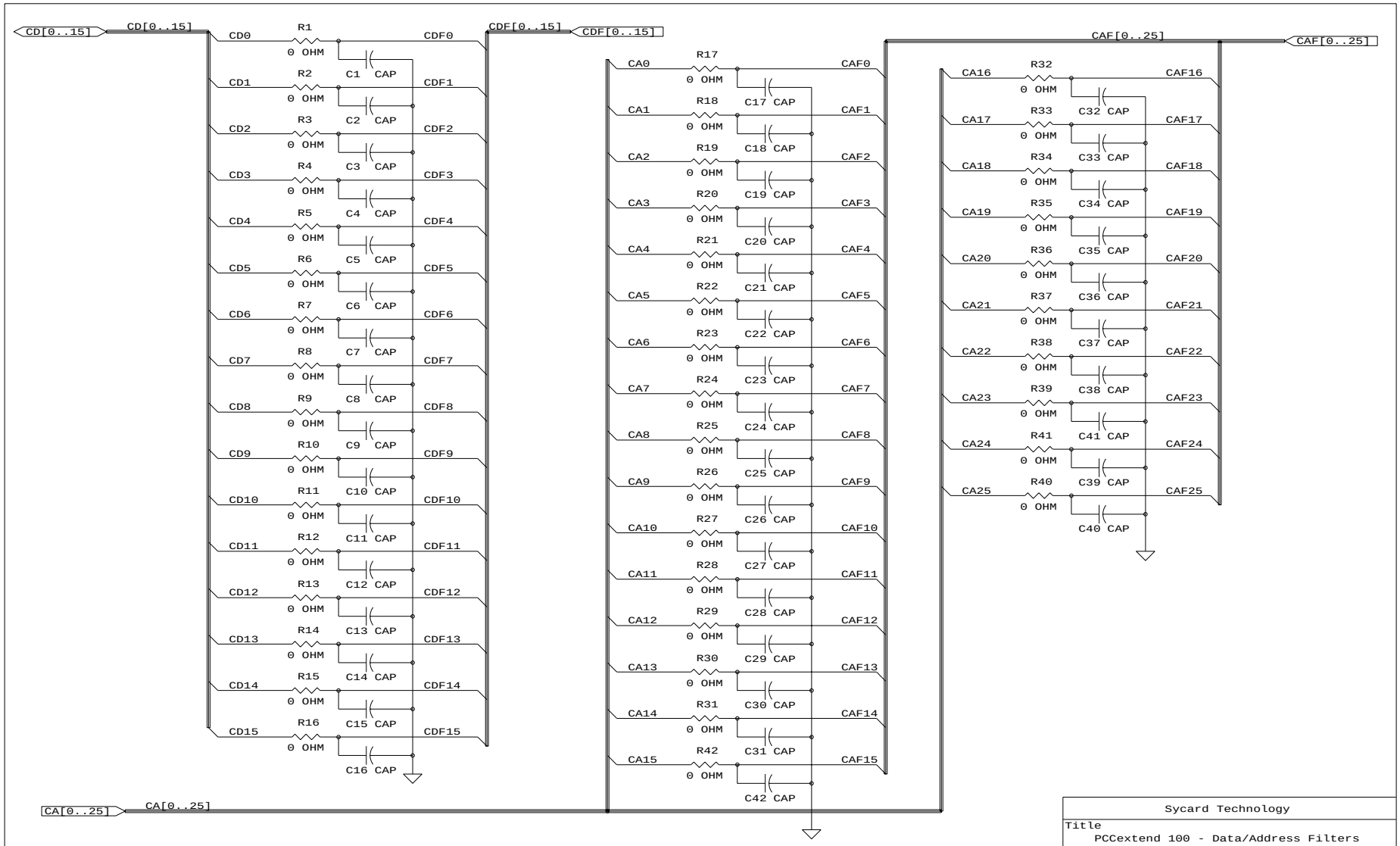

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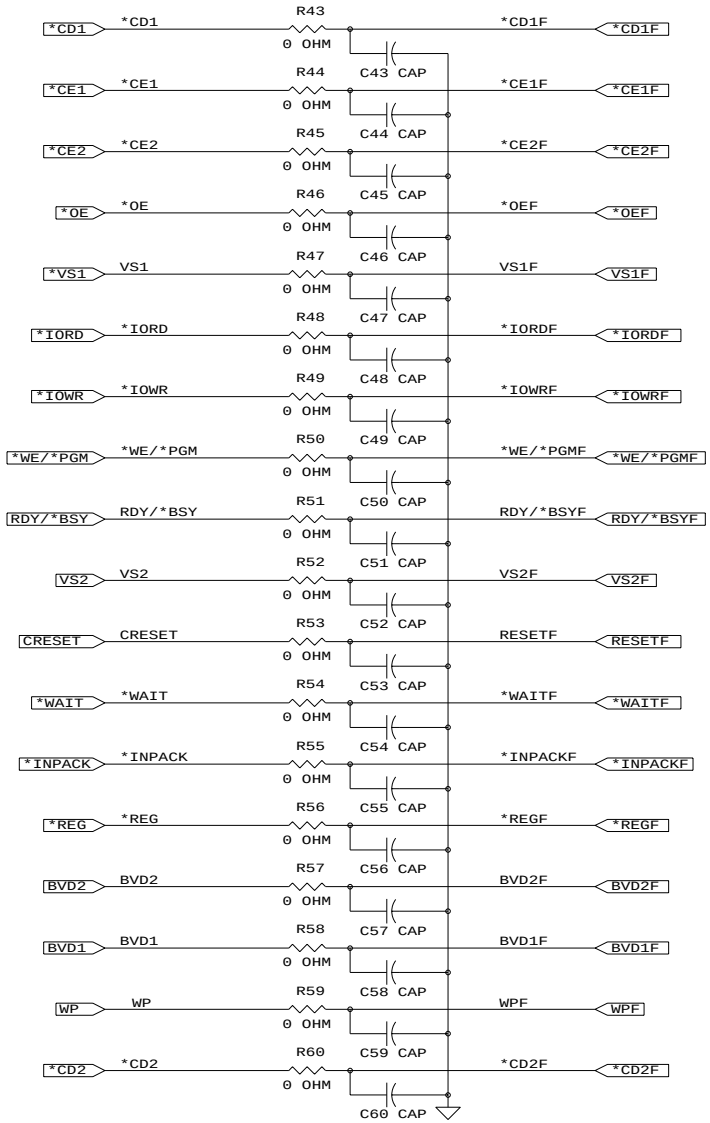

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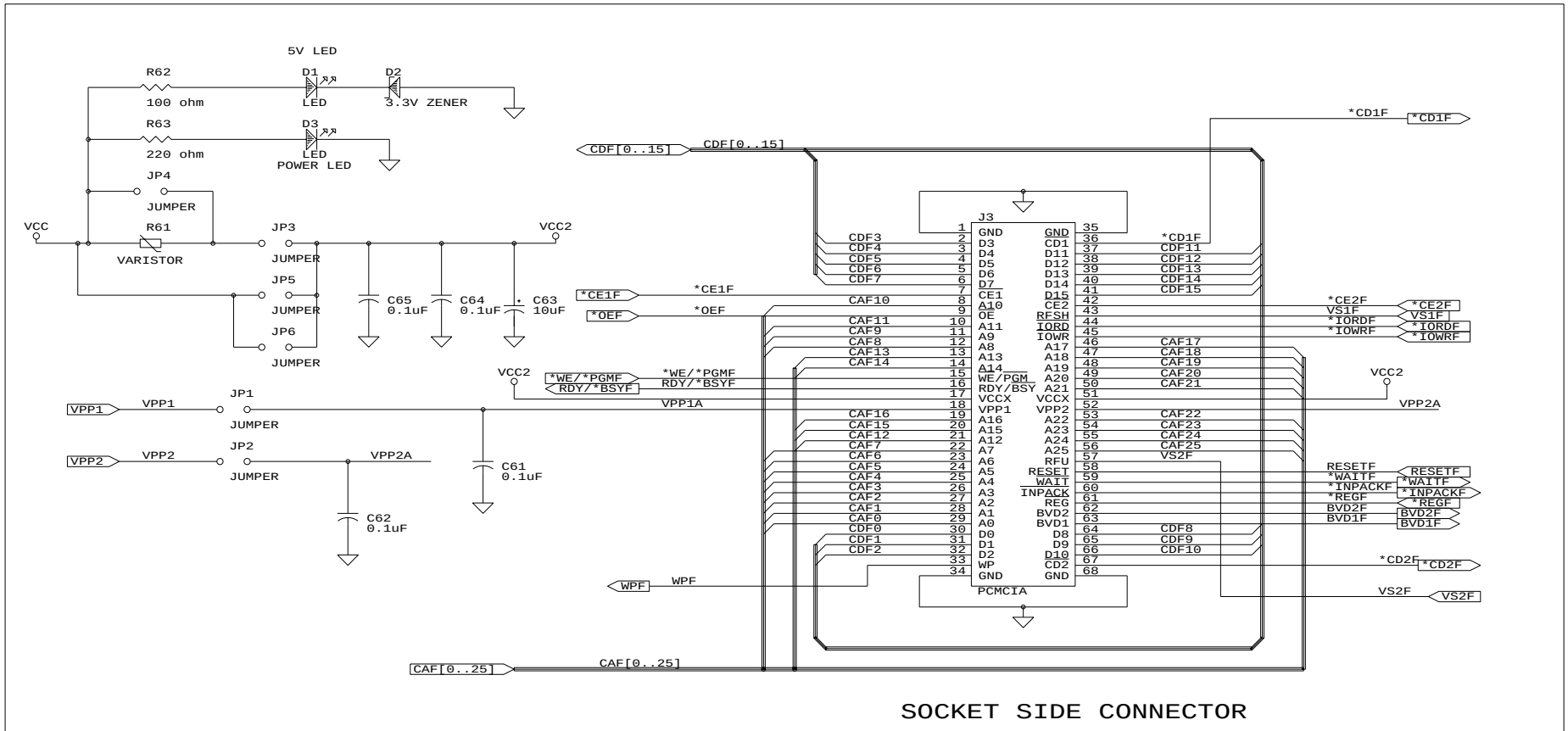

SOCKET SIDE CONNECTOR

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